REMARKS

The application included claims 1, 2 and 42-48 prior to entering this amendment.

The Examiner rejects claims 1, 2 and 42 under 35 U.S.C. § 103(a) as being unpatentable over Busking et al. (U.S. Patent 6,107,684) in view of Gonda (U.S. Patent 4,924,195) and Seshita (U.S. Patent 6,366,770).

The Examiner finds claims 43-48 allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The applicant amends claims 43-48. Claims 49-61 are new. Claims 1, 2, and 42 are cancelled. The application remains with claims 43-61 after this amendment.

The applicant traverses the rejections, adds no new matter, and requests reconsideration.

Specification Amendments

The specification has been amended as requested by the Examiner.

Allowable Subject Matter

The Examiner indicated that claims 43-48 are allowable if rewritten in independent form. Accordingly, claim 43 has been amended to be in independent form, including the elements of independent claim 1 and intervening claim 42. Claims 49 and 50 are new claims dependent on claim 43. Claims 51-58 are new claims including similar elements to claims 43-50. Accordingly, claims 43-58 should be allowable.

Claims 43-48 have been amended to clarify the claims, correct grammatical errors, and correct potential antecedent basis problems. In particular, the terms "etched thereon" and "actually", previously in independent claim 1, have not been added to claim 43 when incorporating the elements of claim 1 into claim 43. In addition, "which" has been changed to "that" in the phrase "that require theoretically negative reactive component values" when incorporated from claim 1 into claim 43.

Claim Rejections - 35 U.S.C. § 103

A. Claim 1

As amended, claim 1 includes "an integrated circuit die having at least one integrated circuit and a first negative-inductance shunt element; and an impedance inverter circuit including the first negative-inductance shunt element, the at least one wire bond, and a second negative-inductance shunt element coupled to the integrated circuit die through the at least one wire bond." Accordingly, the first negative-inductance shunt element is part of both the impedance inverter circuit and the integrated circuit die.

None of Busking, Gonda, and Seshita suggest using a negative-inductance shunt element of an integrated circuit die as part of an impedance inverter circuit. Busking does mention on-chip inductor 8; however, it is used to tune out the parasitic capacitance between pin 1 and the base plate 3, not to provide a negative inductance. Busking, col. 3, ll. 21-23. Furthermore, Busking itself teaches against using such elements because of the increased need for chip area and power. Busking, col. 3, ll. 27-35.

Accordingly, the combination of Busking, Gonda, and Seshita does not teach or suggest each and every element of claim 1 and dependent claims 59-61. The Applicant asserts that claims 1, and 59-61 are allowable over the cited references of record.

B. Claim 59

Claim 59 recites that "at least one of the first negative-inductance shunt element and the second negative-inductance shunt element has a negative inductance only over a limited bandwidth." The only mention of negative inductance in the cited references was in Gonda. Gonda, col. 2, ll. 9-26. However, there is no mention in Gonda of a bandwidth of the negative inductance. Aecordingly, combination of Busking, Gonda, and Seshita does not describe a negative-inductance shunt element having a negative inductance only over a limited bandwidth as described in claim 59. The Applicant asserts that claim 59 and dependent claim 60 are allowable over the cited references of rccord.

C. Claim 61

Claim 51 recites that "the second negative-inductance shunt element is external to the housing." Thus, the impedance inverter circuit includes elements external to the housing. In

contrast, in Busking, Gonda, and Seshita, any elements are either not given a location, or described internal to a package.

For example, in Busking, all references to components are made with respect to locations between a pin 1 and a semiconductor chip 5. Busking, FIGS. 1-4. No mention is made of a component on the opposite side of a pin from the semiconductor chip 5. Similarly, in Seshita, all components are between a pin 4 and a microwave monolithic integrated circuit 10. Seshita, FIGS. 1a-3. Gonda does not mention a package or housing.

Accordingly, the Applicant asserts that claim 51 is allowable over the cited references of record.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 43-58 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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